WHAT IS CLAIMED IS:

1. A fault simulation method for a semiconductor IC, said method comprising the steps of:

generating a test pattern sequence composed of two or more test patterns for input to said semiconductor IC;

performing a logic simulation of the operation of said semiconductor IC in the case of applying thereto each of said two or more test patterns of said test pattern sequence, and calculating a logic signal value sequence in each signal line in said semiconductor IC; and

generating a list of faults, which are detectable by a transient power supply current testing using said test pattern sequence, through the use of said logic signal value sequence in said each signal line calculated by said logic simulation.

2. The method of claim 1, wherein said fault list generating step is a step of generating said fault list for each logic gate in said semiconductor IC.

3. The method of claim 2, wherein said fault list generating step is a step of checking, for said each logic gate, whether a logic signal value sequence in an output signal line of said each logic gate has been changed, and if so, generating said fault list in which an identifier of a test pattern sequence having changed said logic signal value sequence and said logic gate are registered in correspondence with each other.

4. The method of claim 1, wherein said fault list generating step is a step of generating said fault list for said each signal line.

5. The method of claim 4, wherein said fault list generating step comprising the steps of:

checking, for said each signal line, whether said logic signal value

sequence in said each signal line has been changed;

if so, checking whether a logic signal value sequence in an output signal line of a logic gate having its input connected to said signal line, in which said logic signal value sequence has been changed, is changed by a test pattern sequence having changed said logic signal value sequence in said signal line, and if so, generating said fault list in which said signal line and an identifier of said test pattern sequence having changed said logic signal value sequence in said signal line are registered in correspondence with each other.

6. The method of claim 1, wherein said fault list generating step is a step of generating said fault list for each signal propagation path in said semiconductor IC.

7. The method of claim 6, wherein said fault list generating step is a step of checking, for said each signal propagation path, whether logic signal value sequences at respective points in said each signal propagation path have all been changed, and if so, generating said fault list in which an identifier of a test pattern sequence having changed said logic signal value sequences and said each signal propagation path are registered in correspondence with each other.

8. The method of claim 1, further comprising the step of calculating said logic signal value sequence for every test pattern sequence prior to said fault list generating step.

9. The method of claim 1, further comprising the step of calculating said logic signal value sequence and generating said fault list upon generation of each test pattern sequence.

10. A fault simulator for a semiconductor IC, comprising:

test pattern generating means for generating a test pattern sequence composed of two or more test patterns for input to said semiconductor IC;

a logic simulator supplied with said test pattern sequence, for performing a logic simulation of the operation of said semiconductor IC in the case of applying thereto each of said two or more test patterns, and for calculating and outputting a logic signal value sequence in each signal line in said semiconductor IC;

a memory for storing said calculated logic signal value sequence generated in said each signal line for each test pattern sequence; and

fault list generating means supplied with said logic signal value sequence of said each signal line stored in said memory, for generating a list of faults detectable by a transient power supply current testing using said test pattern sequence.

11. A fault simulation method for a semiconductor IC, said method comprising the steps of:

inserting an assumed fault in said semiconductor IC;

generating a test pattern sequence composed of two or more test patterns for input to said semiconductor IC;

applying said test pattern to said semiconductor IC with said assumed fault inserted therein and performing a circuit simulation of the operation of said semiconductor IC to thereby calculate a transient power supply current of said semiconductor IC;

comparing said calculated transient power supply current with the transient power supply current of a normal circuit and deciding whether said assumed fault is detectable by a transient power supply current testing using said test pattern sequence; and

generating a fault list in which said detectable fault and an identifier of said test pattern sequence are registered.

12. A fault simulator for a semiconductor IC comprising:

test pattern generating means for generating a test pattern sequence composed of two or more test patterns for input to said semiconductor IC;

fault inserting means for inserting an assumed fault into said semiconductor IC;

a circuit simulator for applying said test pattern to said semiconductor IC with said assumed fault inserted therein and performing a circuit simulation of the operation of said semiconductor IC to thereby calculate a transient power supply current of said semiconductor IC; and

fault list generating means for comparing said calculated transient power supply current with the transient power supply current of a normal circuit, for deciding whether said assumed fault is detectable by a transient power supply current testing using said test pattern sequence, and for registering said detectable fault and an identifier of said test pattern sequence in a fault list.